ABSTRACT OF THE DISCLOSURE

An ESD protection structure for use in high speed (e.g., 5-7 GHz RF frequency) CMOS and BiCMOS ICs that has a low leakage current and a low equivalent capacitance. The ESD protection structure can be manufactured using conventional processes and includes a semiconductor substrate of a first conductivity type (e.g., a P- epitaxial silicon semiconductor substrate) with a well region of a second conductivity type (e.g., an N- well region) disposed therein. The structure also includes a first region of the first conductivity type (e.g., a P+ first region) disposed in the well region on the semiconductor substrate, as well as a second region of the second conductivity type (e.g., an N+ second region) disposed in and on the semiconductor substrate and spaced apart from the first region. Furthermore, an electrical isolation region is disposed in the semiconductor substrate between the first region and the second region. The ESD protection structure exhibits diode-like electrical behavior with the first region serving as an anode and the second region serving as a cathode, including a low equivalent capacitance and low reverse bias leakage current.